DESIGNING SPACE CUBE 2 WITH ELEGANT FRAMEWORK

Session: SpaceWire test and verification,

Short Paper

Hiroki Hihara

NEC TOSHIBA Space Systems, Ltd., 10, Nisshin-cho 1-chome, Fuchu, Tokyo, Japan

Shuichi Moriyama, and Tatsuya Takezawa

NEC Soft, Ltd., 2-22 Wakaba-cho, Kashiwazaki, Niigata, Japan

Yuji Nishihara

JAXA's Engineering Digital Innovation Center, Japan Aerospace Exploration Agency (JAXA), 2-1-1 Sengen, Tsukuba, Ibaraki, 305-8505, Japan

Masaharu Nomachi

Laboratory of Nuclear Studies, Graduate School of Science, Osaka University,

1-1 Machikaneyama, Toyonaka, Osaka 560-0043

Tadayuki Takahashi, and Takeshi Takashima

Department of High Energy Astrophysics, Institute of Space and Astronautical Science (ISAS), Japan Aerospace Exploration Agency (JAXA), 3-1-1 Yoshinodai, Sagamihara,Kanagawa 229-8510, Japan

E-mail: hihara.hiroki@ntspace.jp, moriyama@mxp.nes.nec.co.jp, takezawa@mxa.nes.nec.co.jp, nishihara.yuuji@jaxa.jp, nomachi@lns.sci.osaka-u.ac.jp, takahasi@astro.isas.jaxa.jp, ttakeshi@stp.isas.jaxa.jp

ABSTRACT

Space Cube 2 is the first SpaceWire based satellite onboard system controller in Japan as well as the first real application of ELEGANT (Electric Design Guidance Tool for Space Use) ELAGANT, which is developed by JAXA (Japan Aerospace Exploration Agency). ELEGANT has the capability of top down design using hardware and software collaborating design methodology. It will realize high quality and rapid design of satellite onboard digital circuits.

The system level specification is modelled as behaviours and channels, which is described in SpecC language at the first step in ELEGANT design flow. Designers don't have to make specific design concerning neither hardware implementation nor software implementation in this phase. The specification model can be verified by simulation subsystem within the specification model simulator. After the specification is verified, designers can evaluate and select among possible architectures assisted by the architecture exploration tool. Evaluation based on processing speed, software execution steps and hardware scale in accordance with several hardware-software partitioning is possible. In consequence, designers can select the most suitable architecture for their project demands. Once the architecture

is fixed, designers don't have to re-design the hardware implementation portion, because the behaviour description written in SpecC is synthesized into HDL (hardware description language) directly with behaviour synthesis tool included in ELEGANT framework. The capacity of synthesized hardware on FPGAs or ASICs are slightly larger than ones which are logically synthesized from hand-coded HDL, and compact enough for space use.

Since SpaceWire is realized in digital implementation, it is one of the most suitable application for system level verification and validation as well as behaviour synthesis.